St. Joseph's Institute of Technology

St. Joseph's Group of Institutions

OMR, Chennai – 119

Department of Electronics and Communication Engineering

(Accredited by NBA)

FACULTY DETAILS

Staff Name:	**Dr.R.NIROSHA**
Designation:	Assistant Professor
Date of Birth:	09-06-1988
Educational Qualification:	M.E.,Ph.D
Area of Interest:	Semiconductor Devices, Healthcare Technology, and Wireless Communication.
Years of Experience:	5 Year & 7 Months
Area of Research:	Semiconductor Devices
No. of Students Project Guided	2
FDP & Workshop Funding	
R & D Activities	
Publications Details	**SCI/SCOPUS INTERNATIONAL JOURNALS** • **Nirosha. R.,** and Rajesh Agarwal. "Dual-Gate Dual-Contact Integrated Silicon Based Organic Thin Film Transistor for Analog and Digital Applications." ***Silicon* 14**, no. 12 (2022): 6661-6677. **Impact Factor: 2.941.** • **Nirosha.R**., and Rajesh Agarwal. "Comprehensive Temperature-Dependent DC Characterization of Organic Thin Film Transistor for Sensing Applications." ***IEEE Sensors Journal* 22.17** (2022): 16794-16803. **Impact Factor:4.325.** • **R. Nirosha** and R. Agarwal, "Microelectronics Reliability" Characterization and modeling of threshold voltage for organic and amorphous thin-film transistors," *Microelectron. Reliab.*, vol. 147, no. June, p. 115054, 2023, doi: 10.1016/j.microrel.2023.115054. **Impact Factor:1.418.** • **Nirosha R.,** and Rajesh Agarwal. "Gate dielectric based steady state & transient analysis of channel characteristics for organic thin-film transistors." *Journal of Materials Science: Materials in Electronics* 34.31 (2023): 2120. **Impact Factor:2.779.** • Singh, A.K., Misra, R., Wadhwa, G., **Nirosha.R** and Agarwal, R.,

	2022, September. Design and Performance Analysis of Partially Depleted and Fully Depleted Silicon on Insulator MOSFET. In ***Journal of Physics****: Conference Series* (Vol. 2335, No. 1, p. 012042). IOP Publishing. **Impact Factor:0.547.** • **R. Nirosha**, Biometric watermarking Techniques in Frequency Domain In **International Journal of Applied Engineering Research.** **PATENT PUBLISHED:** • A patent for **"AN INTEGRATED DUAL-GATE DUAL INSULATING CONTACT (IDGDIC) SILICON BASED ORGANIC THIN FILM TRANSISTOR"** by Rajesh Agarwal and **R. Nirosha** has been published in **Indian Patent Application No. 202241042265 dated 23/07/2022.** **SCOPUS INDEXED INTERNATIONAL CONFERENCES** • Nirosha R, Agarwal R. **Study of Contact Resistance in Amorphous Zinc Oxide Based Thin-Film Transistors**. IEEE 3rd Global Conference for Advancement in Technology (GCAT) 2022 Oct 7 (pp. 1-6). IEEE • R. Nirosha, Rajesh Agarwal, and T. Rama Rao. **Dual-Gate Integrated Organic Thin Film Transistor for Digital Applications**. 1st International Conference of Electronics, Photonics and Smart Technologies (ICePhaST-2020) Vol-1,2020, ISBN 978-93-84136-20-8. (**Received as the "Best Paper Award" ICePhaST-2020**). • R. Nirosha, Aishiki Halder, Rajesh Agarwal, Vaishnavi upendran. **Analysis of the Effect of Different Electrical and Physical Parameters on Contact Resistance in Organic Thin Film Transistors and Optimization Using Machine Learning**. 2nd International Conference on Recent Advances in Electrical, Electronics, Ubiquitous Computational Intelligence (RAEEUCCI-2023). **(PRESENTED) (Received as the "Best paper Award", RAEEUCCI-2023).** 1. Demonstrated a project titled "**Organic Thin Film Transistor**" has won **THIRD** in the project EXPO part of 2nd International Conference on Recent Advances in Electrical, Electronics, Ubiquitous Computational Intelligence (RAEEUCCI-2023).
FDP & Workshop Attended Details	• Industrial applications of embedded systems and IOT between 22/8/24 and 28/8/24 organized by Rajalakshmi Engineering College.

	• Attended a Five Days Summer School on **"Emerging Devices and Circuits to Mimic Biologically Plausible Neuronal Functionalities for Neuromorphic Computing"**, organised by IEEE EDS Student Branch Chapter in association with Department of ECE at **IIITDM, Kancheepuram,** held during 19th-23thDec 2022. • Attended a One Professional Development Hour on **"Compact Models for Circuit Simulation of Component-Level ESD"**, organised by **IEEE Electron Devices Society Delhi Chapter-India** during 25th July 2022. • Attended a STTP on **"Research Opportunities in Semiconductor Materials and Devices" ROSMD-2021** organised by **IIITDM, Kancheepuram,** held on 22-26 October 2021. • Attended a Webinar on **"Semiconductor Device Modelling using Silvaco TCAD"** organized by **Cognitive Design Technology Pvt, Bangalore,** India on 7th May 2021. • Attended a three-day webinar series on **"Solar Cell and Organic Thin Film Transistor for Wearable Applications"** organized by **IE(I), Kattankulathur Local Centre & Department of Electronics and communication Engineering, SRM Institute of Science and Technology** from February 3rd-5th 2021. • Attended a Six Days Faculty Development Programme on **"Recent Advancement in Organic & Nano Electronics RAONE 21"** organized by Department of Electronics and communication Engineering, **SRM Institute of Science and Technology** during 8th- 13th October 2021. • Attended Faculty Development Programme on **"Recent Advancements in Semiconductor Technologies-RASET"** in **SRM Institute of Science and Technology**, on October 9th - 14th 2020
NPTEL Courses	NIL
Professional Membership	Member of IAENG