St. Joseph's Institute of Technology

St. Joseph's Group of Institutions

OMR, Chennai – 119

Department of Electronics and Communication Engineering
(Accredited by NBA)

Staff Name:	Mrs. B. Saraswathy
Designation:	Asst. Professor
Date of Birth:	19-10-1978
Educational Qualification:	M.E, (Ph. D)
Area of Interest:	VLSI design, ASIC Design, Hardware Accelerators, Approximate Computing, Precision Scalable Computing.
Years of Experience:	19 Years 11 Months
Area of Research:	Energy Efficient Multiplier Architectures
Supervisor:	
No. of Students Project Guided	10
Publications Details:	Journals (SCIE- Indexed)- 4, International Conferences- 3
FDP & Workshop Attended Details:	FDP-6 (Inclusive of 2 NPTEL)
Professional Membership:	ISTE

Journal Publications:

1. Saraswathy, B. Anita Angeline, A. (2026). ASIC-based design space exploration of precision-scalable multiplier architectures for edge AI accelerators. Journal of Engineering Research, https://doi.org/10.1016/j.jer.2026.10.061

2. Anand, A., Saraswathy, B., Sasipriya, P., Anita Angeline, A (2026). Design of a low-power RISC-V based intelligent endoscopy detection processor: EndoRISC-V. *Scientific Reports*. https://doi.org/10.1038/s41598-026-55813-1

3. Saraswathy, B. Anita Angeline, A. (2026). Design and analysis of an energy-efficient floating-point logarithmic piecewise approximate multiplier. AEU-International Journal of Electronics and Communications, 156453. https://doi.org/10.1016/j.aeue.2026.156453

4. Saraswathy, B. Anita Angeline, A. (2025). Dynamic-precision configurable multiply-and-accumulate architecture for hardware accelerators. Integration, 103, 102419. https://doi.org/10.1016/j.vlsi.2025.102419

Conference Publications:

1. Saraswathy, B., & Angeline, A. A. (2026, May). Design and Evaluation of Approximate Radix-4 Partial Product Generators for Hardware-Efficient Multiplication. In *2026 International Conference on Next Generation Electronics (NELEX)* (pp. 1-5). IEEE. https://doi.org/10.1109/NELeX69209.2026.11590314

2. Bharadhwaj, S. A., Joshittha, K., Saraswathy, B., Sasipriya, P., & Angeline, A. A. (2026, May). Hardware Implementation of Deep Neural Network Using Various Multipliers. In *2026 International Conference on Next Generation Electronics (NELEX)* (pp. 1-6). IEEE. https://doi.org/10.1109/NELeX69209.2026.11590066

3. Ramasubramanian, V., Heshwar, A. S. N., Srikrishnan, G., Saraswathy, B., Sasipriya, P., & Anita Angeline, A. (2025, June). Implementation of Neuron Design with Different Activation Functions on FPGA. In *2025 Second International Conference on Cognitive Robotics and Intelligent Systems (ICC-ROBINS)* (pp. 89-93). IEEE. https://doi.org/10.1109/ICC-ROBINS64345.2025.11086235